AMENDMENT TO THE CLAIMS

1. (Currently amended) A method for testing an integrated circuit (IC) comprising:

selecting a bit during an ABIST test from each of a plurality of memory arrays formed on an IC chip;

selecting one of the plurality of memory arrays on the IC chip; and

storing the selected bit from the selected memory array in a component of the IC chip wherein an outcome of the ABIST test is determined based on the stored selected bit.

2. (Original) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays includes selecting a wordline in each of the plurality of memory arrays.

3. (Original) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays includes overwriting an initial state bit value of a selection circuit with a value of the selected bit.

4. (Original) The method of claim 1 wherein storing the selected bit from the selected memory array includes storing the selected bit from the selected memory array in a latch.

5. (Original) The method of claim 4 wherein storing the selected bit from the selected memory array includes one of storing an initial state bit value of an output of a selection

circuit and storing a modified initial state bit value of the output of the selection circuit in the latch.

6. (Previously presented) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays formed on an integrated circuit chip, selecting one of the plurality of memory arrays, and storing the selected bit from the selected memory array are performed during an ABIST test of the integrated circuit chip.

7. (Currently amended) A method for testing an integrated circuit (IC) comprising:

selecting a bit during an ABIST test from each of a first and second plurality of memory arrays formed on an IC chip;

selecting one memory array from each of the first and second plurality of memory arrays of the IC chip; and

storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays in a component of the IC chip wherein an outcome of the ABIST test is determined based on the stored selected bit.

8. (Original) The method of claim 7 wherein selecting a bit from each of the first and second plurality of memory arrays includes selecting a wordline in each of the first and second plurality of memory arrays.

9. (Original) The method of claim 7 wherein selecting a bit from each of the first and second plurality of memory arrays

includes:

overwriting a first initial state bit value with a value of the selected bit from the selected memory array of the first plurality of memory arrays; and

overwriting a second initial state bit value with a value of the selected bit from the selected memory array of the second plurality of memory arrays.

10. (Original) The method of claim 7 wherein storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays includes:

storing the selected bit from the selected memory array of the first plurality of memory arrays in a first latch; and

storing the selected bit from the selected memory array of the second plurality of memory arrays in a second latch.

11. (Original) The method of claim 10 wherein storing the selected bit from the selected memory array of the first plurality of memory arrays includes one of storing an initial state bit value of an output of a first selection circuit and storing a modified initial state value of the output of the first selection circuit in a first latch; and

wherein storing the selected bit from the selected memory array of the second plurality of memory arrays includes one of storing an initial state bit value of an output of a second selection circuit and storing a modified initial state value of the output of the second selection circuit in a second latch.

12. (Previously presented) The method of claim 7 wherein selecting a bit from each of a first and second plurality of memory arrays formed on an IC chip, selecting one memory array from each of the first and second plurality of memory arrays, and storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays are performed during an ABIST test of the IC chip.

13. (Previously presented) An apparatus comprising:

a plurality of memory arrays;

a latch;

a selection circuit coupled to the plurality of memory arrays and to the latch, and adapted to:

receive a bit from each of the plurality of memory arrays;

select one of the plurality of memory arrays; and

store the bit from the selected memory array wherein an outcome of the ABIST test is determined based on the stored selected bit.

14. (Original) The apparatus of claim 13 further comprising a decoder coupled to the selection circuit.

15. (Previously presented) The apparatus of claim 14 wherein the decoder is adapted to generate signals used to select one of the plurality of memory arrays.

16. (Original) The apparatus of claim 13 wherein the selection circuit comprises a multiplexer.

17. (Previously presented) An apparatus comprising:

a first plurality of memory arrays;

a first latch;

a first selection circuit coupled to the first plurality of memory arrays and to the first latch, and adapted to:

(a) receive a bit from each of the first plurality of memory arrays;

(b) select one of the first plurality of memory arrays; and

(c) store the bit from the selected one of the first plurality of memory arrays wherein an outcome of the ABIST test is determined based on the stored selected bit;

a second plurality of memory arrays;

a second latch;

a second selection circuit coupled to the second plurality of memory arrays and to the second latch, and adapted to:

(d) receive a bit from each of the second plurality of memory arrays;

(e) select one of the second plurality of memory arrays; and

(f) store the bit from the selected one of the second plurality of memory arrays.

18. (Original) The apparatus of claim 17 further comprising a decoder coupled to the first and second selection circuits.

19. (Previously presented) The apparatus of claim 18 wherein the decoder is adapted to generate signals used to select one memory array from each of the first and second plurality of memory arrays.

20. (Original) The apparatus of claim 17 wherein the first and second selection circuit comprise multiplexers.

21. (Previously presented) The apparatus of claim 17 wherein the first and second selection circuits are adapted to perform (a)-(c) and (d)-(f) simultaneously.